Founder review required before broad outreach. Do not add uncited statistics or accreditation claims.

Silicon Chip Verification Skills-Gap Report

A one-page curriculum and skills reference for educators, clubs, and community partners

Problem statement

Many electrical and computer engineering programs introduce digital logic and hardware description language (HDL) concepts. Industry verification work, however, asks for more than familiarity with syntax: simulation discipline, testbench habits, debugging evidence, and a progression into SystemVerilog and UVM-oriented practice.

The gap is not a lack of interest. It is often a gap between introductory HDL exposure and the habits teams use to show that a design behaves as intended.

Curriculum-to-industry framing

Typical ECE / computer engineering pathways emphasize theory, digital fundamentals, and selected HDL exposure. Time and lab constraints mean many courses cannot fully cover modern verification workflows.

Industry entry conversations frequently look for signals that a learner can:

- write and simulate RTL with intention;
- build or extend a testbench;
- explain failures with evidence;
- move from Verilog foundations toward SystemVerilog and structured verification practice.

This report is a **curriculum and skills reference**, not an accreditation map, ranking, or adoption claim.

Verification-skills progression

A practical skills sequence for discussion and self-directed practice:

Verilog → SystemVerilog → UVM → Advanced Verification

1. **Verilog** — foundational RTL expression, simulation basics, and debugging habits.
2. **SystemVerilog** — stronger modeling and verification constructs used in contemporary flows.
3. **UVM** — reusable verification structure and methodology awareness for larger environments.
4. **Advanced verification** — deeper coverage, assertion, and evidence-oriented practice as roles demand.

Foundational RTL work is the on-ramp. Later verification capability depends on early habits: readable code, simulation evidence, and explaining what passed or failed.

Industry and workforce context

Semiconductor design and verification remain specialized domains where practice and proof matter. Public policy conversations in several regions have also increased attention to domestic semiconductor capability and technical workforce development.

Review note (founder): Do not add quantitative workforce percentages, salary claims, placement rates, or legislative outcome claims in this report unless a primary source is cited with access date and the founder has approved the wording. Prefer qualitative framing until reviewed sources are attached.

Selected public context placeholders for founder-approved citation:

Topic	Suggested source class	Status
Semiconductor workforce attention	Government / agency workforce or CHIPS-related public materials	Citation pending founder approval
Verification skill expectations	Industry society or vendor education materials (IEEE, SEMI, tool vendors)	Citation pending founder approval

How to use this report

- Share as a one-page discussion aid with student clubs, faculty contacts, or community organizers.

- Use the progression as a shared vocabulary for curriculum conversations.
- Point interested learners to free SkillLift.org context first; route structured practice to SkillLift.io when appropriate.
- Do not present this page or PDF as evidence of university adoption, employer endorsement, or formal partnership.

SkillLift pathway (neutral)

- **SkillLift.org** — free public explainers, curated resources, and partner kits. Explains, curates, and routes. No learner account or lead capture required to browse.
- **SkillLift.io** — structured practice, readiness diagnostic, and proof surfaces. Teaches, verifies, and hosts interactive learning.

Cold partner pathway (tracked): SkillLift.io Silicon Chip readiness diagnostic

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